UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,151	08/04/2003	Masashi Kiyose	10449-070001 / P1S2003116	5105

26161 7590 07/12/2004

FISH & RICHARDSON PC
225 FRANKLIN ST
BOSTON, MA 02110

EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,151	KIYOSE ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,3,4,6,8,10,11,13,15 and 17 is/are rejected.

7)☒ Claim(s) 2,5,7,9,12,14 and 16 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 04 August 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-4, 8, 10-11 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,363,419, issued to Ho.

As per claim 1, Ho discloses a PLL circuit (Fig. 2) for use with first (REF FREQ on line 23 to the phase detector 12) and second (the signal output from the divide-by-16 circuit 14) reference signals, the cycle of the second reference signal being longer than that of the first reference signal (as shown, the cycle of the second reference signal is 16 times longer than the first reference signal), the PLL circuit comprising:

a voltage controlled oscillator (the combination of circuits 3 and 4) for generating a clock signal (at the output of VCO 4) in accordance with a control voltage (the signals on lines 5, 6' and 7'), and the clock signal having a phase and frequency (because the circuit 4 is an oscillator);

a first loop (the upper loop) for controlling the frequency of the clock signal in accordance with the first reference signal (REF FREQ, the functional recitation is met because the upper loop is a PLL); and

a second loop (the lower loop) for controlling the phase of the clock signal in accordance with the second reference signal (because the lower loop is also a PLL) with the second loop generating the control voltage at a constant value (the constant voltage V is supplied by the source voltage V) and supplying the VCO with the constant control voltage until the difference between the frequency of the first reference signal and the frequency of the clock signal converges to within a predetermined range (the control line 6' goes HI, FET 21 is ON when the frequency is out of a predetermined range, column 3, lines 8-19), and thereafter the second loop generating control voltage at a level in accordance with the difference between the phase of the second reference signal and the phase of the clock signal (coarse mode operation, column 2, lines 56-68) and supplying the VCO with the control voltage at the level in accordance with the phase difference.

As per claim 3, the recited first input terminal reads on the terminal on line 5, receiving the first control voltage VA; the recited second input terminal reads on the terminal on line 6' which receives the second control voltage 6'; the recited ring oscillator reads on VCO 4 (column 5, lines 25-26); the functional recitations on the last ten lines are already discussed in claim 1.

As per claim 4, the recited phase comparator reads on phase detector 12, the recited charge pump is disclosed in column 4, lines 31-33 which is pumping charge with variable capacity depending on the difference between the two recited signals.

As per claim 8, this claim is rejected for the same reasons noted in claim 1. The recitation in the preamble section is given no patentable weight because it is merely an intended use and it is not needed to give life and meaning to the body of the claim .

As per claims 10-11, these claims are rejected for the same reasons noted in claims 3-4, respectively.

As per claim 15, this claim is merely a method to operate a PLL circuit having the structure recited in claim 1, since Ho teaches the circuit, he inherently teaches the recited method.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,363,419, issued to Ho.

As per claim 6, Ho discloses a PLL circuit having the structure discussed in claim 1 herein above, and further, Ho discloses the first loop includes a first divisional circuit (11) with a first divisional ratio *n* connected as recited, the functional recitation on the last ten lines of the second loop is also discussed in claim 1.

Ho does not explicitly disclose the second loop include a second divisional circuit connected to the VCO as called for in the claim.

The examiner takes Official Notice the fact that including a divider circuit in the feedback loop of a PLL circuit is old and well-known in the art. The purpose is for reducing the frequency of the feedback signal so that the other circuits in the PLL loop do not have to operate in a high frequency enviroment, and therefore, reducing the potential EMI problem caused by high frequency of oscillating.

It would have been obvious to one skilled in the art at the time of the invention was made to include a second divisional circuit in the second loop of the Ho's PLL circuit for the motivation would be to reduce the potential EMI problems.

As per claims 13 and 17, these claims are rejected for the same reasons and motivation discussed in claim 6.

Allowable Subject Matter

4. Claims 2, 5, 7, 9, 12, 14 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 2 is allowable because the prior art of record fails to disclose or suggest the inclusion of a voltage generation section and a decoder in the second loop.

Claim 5 is allowable because the prior art of record fails to disclose or suggest the inclusion of rising edge, falling edge phase comparators, first and second charge pumps.

Claim 7 is allowable because the prior art of record fails to disclose or suggest the inclusion of a phase comparator and a charge pump in the second loop.

Claims 9, 12, 14 and 16 are allowable for the same reasons noted in claims 2, 5, 7 and 2, respectively.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7/8/04

Minh Nguyen
Primary Examiner
Art Unit 2816